CSC 714 Real Time Computer Systems Project

Pipeline and Path analysis for Power aware Embedded architecture

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Progress Report

The current objective of the project is to use the existing framework for timing analysis and use it with a different ISA. Currently the timing analyzer works with the microsparc architecture and it is being ported to the ISA used by the Simplescalar toolset.

Solved issues-

1) A software patch that uses a PISA assembly file as an input and gives input files for the static cache simulator and the timing analyzer is ready.

2) The timing analyzer has been modified to work with the SimpleScalar ISA.

Next Steps-

1) Currently the data cache simulator is offline. The timing predictions can be made tighter if it can be incorporated into the timing analyzer.