EDF-DVS Scheduling on the IBM Embedded PowerPC 405LP

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OBJECTIVE

Develop an infrastructure for enabling EDF-DVS scheduling on the IBM embedded PowerPC 405LP.

MOTIVATION

Energy management has been a hot issue in embedded systems for a long time. Battery operated mobile devices are becoming more popular than ever, and user expectations and demands on these devices are also growing. Being operated by batteries which have limited energy budget places stringent restrictions on power consumption in such devices, and makes energy conserving a must rather than a convenience. One especially attractive technique for extending battery life is dynamic voltage scaling (DVS). DVS dynamically scales down (or up, depending on the computation demand of the system) the supply voltage of the device's processor. Reducing the supply voltage results in a lower maximum transistor switching speed, which also requires lowering the clock frequency of the device. Assuming that voltage and frequency are linearly related, scaling down both voltage and frequency results in cubic reduction of power consumption.

DVS algorithms have been intensively researched upon for both non real-time and real-time systems. In the case of real-time systems, the DVS algorithm must calculate a safe operation frequency that provides just enough processor computation power to finish a given task before its deadline. The goal is to save the maximum possible amount of energy and yet maintain safe operation of the hard real-time system where all tasks are guaranteed to meet their deadlines.

In this project, we plan to implement a DVS algorithm for a real-time system using IBM's PowerPC 405LP as a substrate. The 405LP processor provides the hardware support required for DVS, and allows software to scale voltage and frequency through user defined *operation points* ranging from a high end of 380 MHz @ 1.8 V to a low end of 152 MHz @ 1 V.

We plan to implement a real-time earliest deadline first (EDF) scheduling policy as part of a user-level threads package under the supported Linux operating system. Then, we will extend the capabilities of the infrastructure to support some popular hard real-time software DVS techniques that leverage the already available hardware DVS support in the PowerPC processor.

TARGET SYSTEM AND TOOLS

The target system is the IBM PowerPC 405LP. This processor is especially attractive for DVS since it has the ability to execute instructions even when the frequency/voltage is being changed.
We are currently investigating the Linux support available for user-level thread management.
We plan to use multimeters to measure voltage changes and oscilloscopes to measure energy/power consumption.

POTENTIAL ISSUES

The PowerPC 495LP runs on Linux. To the best of our knowledge, Linux does not have EDF support. So, the first step is to implement an EDF scheduler on the 405LP Linux O/S.

The 405LP does not include a traditional BIOS, therefore control of the dynamic power state of the system must be implemented in the operating system. There should be at least two voltage levels to choose from; otherwise power consumption can be estimated from the frequency scaling part. There exists a command line tool that can change the frequency as well as voltage.

The DVS scheduling is independent of task scheduling, i.e., the scheduler can be envisioned to be comprised of (1) EDF scheduling and (2) DVS scheduling. These two components are mutually exclusive and independent. This means that even though we plan to identify and implement a specific DVS algorithm, our scheduler will work with any existing DVS algorithm as well.

We propose to implement a EDF and DVS algorithm on the user level and analyzing the power benefits. For initial and preliminary "power benefits" analysis, we plan to develop a simulation model with dummy tasks to and the EDF-DVS scheduler on this model. Once satisfactory results are obtained and time permitting, we intend to make our EDF-DVS scheduler run real tasks, e.g. mpeg player etc.

PROPOSED APPROACH

The major objective of this project is to create a basic infrastructure for investigating hard real-time DVS schemes on the IBM PowerPC 405LP. Task scheduling will be performed on an earliest-deadline-first (EDF) basis.

We plan to create a user-level threads package that provides generic APIs for use by EDF/DVS schedulers. The user-level library will be responsible for thread creation and management and will also have primitives to dynamically change the frequency and voltage. We plan to implement these primitives by studying the source code of an existing command level tool that can change the frequency/voltage dynamically. The threads library will also provide timers that can be set by the scheduler application to emulate task releases.

The EDF scheduler itself will be executed on one of the threads, as also the DVS scheduler. We plan to implement a lightweight (low overhead) EDF scheduler. The framework will be flexible enough to allow any scheduling algorithm and also any DVS algorithm.

We are also interested in performing some hardware characterization of the IBM 405LP in terms of quantifying the latency of frequency/voltage switching and the code throughput that is achieved during the transition.

We plan to compare the performance of various EDF-DVS algorithms against a base machine that does plain EDF. We plan to compare the actual frequency/voltage profile of the EDF-DVS schemes with the base scheme (constant frequency/voltage). We are also interested in measuring the power/energy consumed using an oscilloscope (if time permits).

DELIVERABLES

1. Webpage: A webpage to report progress and to present important milestones and results. The webpage can be found at www4.ncsu.edu/~aaelhaj/714/project.htm

2. Software: Commented source code of the threads package and various EDF-DVS scheduler implementations.

3. Demonstration: We will demonstrate our implementation of select EDF-DVS algorithms on the IBM PowerPC 405LP.

4. Technical Documentation: A detailed technical documentation of third-party software installed and detailed description of our software packages and project report.

HARD REAL-TIME DEADLINES [;)]

03/25: Proposal submission
03/29: Investigate
    Available tools for power management in power pc
    Linux support for user-level threads
04/03: Half way through implementing threads library, EDF/DVS application threads, setting up the hardware.
04/07: Submit mid-semester report and update webpage
04/11: Complete basic EDF-DVS schedulers; Creating synthetic benchmarks
04/15: Complete threads library package.
04/20: Complete testing on synthetic benchmarks and start looking at actual real-world workloads (time permitting).
04/27: Submit final report

PROJECT WEBSITE

http://www4.ncsu.edu/~aaelhaj/714/project.htm

REFERENCES

K. Nowka, G. Carpenter and B. Brock. The Design and Application of the PowerPC 405LP Energy-Efficient System on Chip. IBM Journal of Research and Development, Vol. 47, NO. 5/6, September/November 2003.

IBM and MontaVisa Software. Dynamic Power Management for Embedded Systems. Whitepaper available online at http://www.research.ibm.com/arl/papers/DPM_V1.1.pdf.

B. Brock and K. Rajamani. Dynamic Power Management for Embedded Systems. Proceedings of the IEEE International SOC Conference. September 2003.