CSC 714 Project Proposal

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"Study of leakage on an IBM PowerPC 405LP Embedded Processor and ways to reduce energy consumption, by combining sleep and low-power modes."

Project URL: http://www4.ncsu.edu/~nsdeshpa/project.html

Abstract

Techniques like dynamic voltage scaling (DVS) are instrumental in reducing the energy consumption occurring in an embedded processor. On the other hand, sleep modes eliminate all power consumption, static as well as dynamic. I propose to combine the benefits of both techniques, and study the effects of the combination on overall energy consumption in the processor.

System Description

For experimentation, an IBM PowerPC 405LP test-board has been provided, on which MontaVista Linux 3.0 has been installed as the RTOS. The board is connected to a PC via Ethernet as well as through a serial port. A data acquisition board, called "comedi" is responsible for voltage, current and power measurements and reporting it to the PC. A program, called "Beech" uses all the raw data obtained from the "comedi" board and handles it logically to be displayed on the PC screen. Another program, "avg" displays the average power consumed in mWatts during the measurement period.

To test each mode manually, we firstly specify a wakeup time to a file called pm_alarm on the board, which communicates the wakeup time to the Advanced Power Management (APM) section of the PowerPC, which in turn generates a wakeup interrupt at the time specified. The system is then put to sleep, and it wakes up at the desired time. The overhead between wakeup and fully-active states is then measured, and reported. This overhead enables us to then decide the efficiency of the sleep mode to be used for further experimentation.

Project Outline

The DVS part of the project has already been implemented and is in place, where one gets to experiment with different kinds of DVS algorithms, by specifying the algorithm to be used, the size of the task set, the WCET Utilization, etc. My task is to work on the memory leakage part of the project, in which the significant steps are:

1. Finding out the different sleep modes supported by the processor.
2. After identifying the sleep modes, testing them all out one by one and then finding out which mode is the best to use for further experiments by seeing the power consumed during each mode.
3. On the basis of this, we select a mode and then find out the sleep overhead, i.e. how much time the system takes to go from the "asleep" to the "full-awake" status.
4. Initially, the sleep overhead measurements will be at "second" granularity. This overhead can be measured using functions like setitimer(), which will set a periodic timer, that will produce an interrupt every second. A signal handler will be installed using sigaction() that will handle the timer interrupt produced by setitimer().
5. This needs to be improved to millisecond or even microsecond granularity in the later stages, so that experimentation can be done.
6. Study the overhead of accessing sleep modes through the /proc file system v/s a regular system call. Depending on the outcome, we may or may not use the system call functionality.
7. After this, we integrate the sleep mode with DVS to study how energy consumption and leakage is affected and the trade-offs between using DVS and sleep modes.

References:

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