

CSC714 - Project proposal

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Power-Constrained Real Time Scheduling

<http://www4.ncsu.edu/~xluo6/poweraware.html>

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Abstract

In this project, we intend to design and simulate a power-constrained real time scheduling scheme. The scheduling schemes discussed so far in class ensure timely completion of jobs but they are oblivious to power consumption. Today with the advent of small-sized computing systems and SoCs, power management is of high importance. In this work we intend to make the existing scheduling schemes power-aware so that they can minimize power consumption while respecting the required deadlines.

Motivation

Today we have an array of portable battery operated devices that need real time guarantees. Due to their dependence on batteries for power supply, there is a constraint on the possible peak power consumption. We call these power constrained systems. Minimizing power consumption helps lengthening the battery life. High power consumption is accompanied by high heat dissipation which in turn translates into high cooling costs. Every penny spent on cooling is every penny not spent on doing work (computing). Hence, powerawareness is critical.

Previous work suggests that for most applications the processor consumes most of the energy that is consumed by the system. Under peak load it consumes nearly 60% of the total energy consumed by the system. Hence, appropriate scheduling of this power hungry resource is critical.

Problem Statement

Given a finite power budget, determine whether a task set is schedulable. If a task set is schedulable, schedule the jobs in such a way that the power consumption in a hyperperiod is minimal and each of the jobs meets its deadline.

Assumptions

We consider only periodic tasks with periods equal to their deadlines. These tasks are independent of each other and are preemptable.

Challenges / Design Issues

There are various possible mechanisms used in the previous work on power savings like forcing the processor into sleep mode, scaling down the processor voltage and frequency to the lowest level. We need to decide whether we choose to include any of these mechanisms in our power model.

Dynamically changing power level demands recalculation of WCET of tasks for that power level. Also we need to perform schedulability test online at each power modulation point. This may add to the scheduling overhead.

Speed reduction and task delaying are two approaches listed in the previous work. Third possible approach could be to force a job to finish its execution as soon as it can with the given power budget. We need to decide which of these or what combination of these approaches would be most appropriate.

Milestones

Week 1 - Complete the literature survey (Neha and Xiaoqing)

Week 2 - Decide upon an appropriate power model that helps us express WCET of the tasks in terms of power. Formulate a schedulability test for power-constrained EDF(Neha) and power-constrained RM(Xiaoqing)

Week 3 - Design power-constrained EDF(Neha) and power-constrained RM(Xiaoqing) by incorporating the power constraint in the vanilla algorithms.

Week 4 - Build a simulator for the two schemes listed above.

Inputs : Tasks T_i (P_i , C_i) and power constraint P_i that should be met

Output: Schedulability \rightarrow Yes or No

Schedule with Timeline and powerline

Week 5 - Debugging and experimentation.

Week 6 - Presentation and final report submission.

References

- DVSleak: Combining Leakage Reduction and Voltage Scaling in Feedback EDF Scheduling (<http://moss.csc.ncsu.edu/~mueller/ftp/pub/mueller/papers/lctes07.pdf>)
- Real-Time Dynamic Voltage Scaling for Low-Power Embedded Operating Systems, P. Pillai and K. Shin, Symposium on Operating Systems Principles'01
- Effective Dynamic VoltageScaling through CPU-Boundedness Detection, C.-H. Hsu and W.-C. Feng, in Proceedings of the 4th International Conference on Power-Aware Computer Systems, ser. PACS'04, 2005
- Memory Access Aware on-line Voltage Control for Performance and Energy Optimization, X. Chen, C. Xu, and R. Dick, in Computer-Aided Design (ICCAD), 2010 IEEE/ACM International Conference on, 2010, pp.365–372.