Report 2

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Tasks accomplished:

1. Modify the DraMon code and run it on the ARC.

2. Get a study on the PCI register and the document of "BIOS and Kernel Developer's Guide (BKDG) For AMD Family 10h Processors".

3. Make clearly about the algorithm how to calculate the NodeID, channel number, Rank, Bank, Row, Column

4. Do the experiment and collect some data.

Result:

In the experiment, I found that the physical address is grouped by the NodeID.

For ARC, There are 4 nodes (memory controllers) in one CPU. Each node (memory controller) has different physical address range.

Node 0:0x0~~0x227FFFFFF

Node 1:0x228000000~~0x427FFFFFF

Node 2:0x428000000~~0x627FFFFFF

Node 3: 0x628000000~~0x827FFFFFF

There are 16 cores in one CPU. When one core in the CPU accesses the main memory, it will access different memory controller and get the different access latency. The following experiment data shows the variable access latency due to the core access different node (memory controller).

Virtual address : 0x2B82002EB010

Physical address: 0x1DAF32010,

Node: 0, channel: 1, rank: 3, bank: 2, row: 6959, column: 512

latency: 8111us

Virtual address : 0x2B82FE2ED010

Physical address: 0x2055BE010,

Node: 0,channel:0, rank: 3, bank: 3, row: 15829, column: 2560

latency: 12466us

Virtual address : 0x2B8535AEF010

Physical address: 0x611485010,

Node:2,channel: 1, rank: 2, bank: 0, row: 16020, column: 2304

latency: 17152us

Virtual address : 0x2b85f8af0010

Physical address: 0x556E74010,

Node: 2, channel: 1, rank: 3, bank: 6, row: 4846, column: 2048

latency: 17006us

Virtual address : 0x2b86f7af1010

Physical address: 0x80ED03010,

Node: 3, channel: 1, rank: 2, bank: 0, row: 7789, column: 768

latency: 16957us

The data clearly shows that the latency from accessing different memory controller. For example, if the core access node 0 (memory controller id 0) will get the least latency. However, if it accesses the node 2 or node 3, there will be more latency.

Next step:

Try to design the new algorithm of virtual address to physical address mapping. Using this new algorithm, we can assign the proper physical address to each program and we can get the memory access latency exactly.